In the Claims:

1. (Currently Amended) An integrated circuit comprising:

a first substantially planar dielectric layer;

first conductive lines on a first level and located in said first dielectric layer;

a second substantially planar dielectric layer formed over said first dielectric layer;

second conductive lines on a second level and located in said second dielectric layer; and

at least one of said ~~the~~ first conductive lines or said second conductive lines comprising ~~comprises~~ a non-rectangular shaped cross-section.

2. (New) The integrated circuit of claim 1 wherein both said first conductive liens and said second conductive lines have a non-rectangular cross-section.

3. (New) The integrated circuit of claim 2 wherein said cross-section of said first and second conductive lines is triangular.

4. (New) The integrated circuit of claim 2 wherein said cross-section of said first and second conductive lines is trapezoidal.

5. (New) The integrated circuit of claim 3 wherein the uppermost portion of said conductive lines on said first level is below the lowermost portion of said conductive lines on said second level.

6. (New) The integrated circuit of claim 2 wherein the uppermost portion of said conductive lines in said first level is co-planar with the lowermost portion of said conductive lines in said second level.

7. (New) The integrated circuit of claim 1 wherein at least one sidewall of said non-rectangular shaped cross-section is non-vertical.

8. (New) The integrated circuit of claim 2 wherein at least one sidewall of said non-rectangular shaped cross-section is non-vertical.

9. (New) The integrated circuit of claim 1 wherein the conductive lines comprise a conductive material selected from a group consisting of aluminum, copper or alloys thereof.

10. (New) The integrated circuit of claim 1 wherein the pitch between adjacent first conductive lines and between adjacent second conductive lines is less than 2F.

11. (New) An integrated circuit comprising:

first conductive parallel lines on one level separated by a selected pitch;

second conductive parallel lines on another level separated by said selected pitch and having a non-rectangular shaped cross-section such that said first and second said conductive parallel lines may be arranged to reduce capacitance between said first and second conductive parallel lines at said selected pitch.

12. (New) The integrated circuit of claim 11 wherein said first conductive parallel lines have a rectangular cross-section.

13. (New) The integrated circuit of claim 11 wherein said first conductive parallel lines have a non-rectangular cross-section.

14. (New) The integrated circuit of claim 13 wherein said cross-sectional shape of said first and second conductive parallel lines is triangular shape.

15. (New) The integrated circuit of claim 14 wherein said one level is a lower level and said another level is an upper level, wherein the vertex of said triangular cross-sectional conductive parallel lines on said lower level points toward said second level and wherein the vertex of said triangular cross-sectional conductive parallel lines on said upper level points toward said lower level.

16. (New) The integrated circuit of claim 15 wherein the vertexes of said conductive parallel lines on said lower level is co-planar with the vertexes of said conductive parallel lines on said upper level.

17. (New) The integrated circuit of claim 15 wherein the vertexes of said conductive parallel lines on said upper level are spaced a selected distance vertically from the vertexes of said conductive parallel lines on said lower level.

18. (New) The integrated circuit of claim 11 wherein said conductive parallel lines on said another level have first and second sidewalls and wherein at least one of said first and second sidewalls is non-vertical.

19. (New) The integrated circuit of claim 13 wherein said cross-section shape of said first and second conductive parallel lines is trapezoidal shaped.

20. (New) The integrated circuit of claim 2 wherein said one level is a lower level and said another level is an upper level.

21. (New) The integrated circuit of claim 2 wherein said one level is an upper level and said another level is a lower level.

22. (New) The integrated circuit of claim 18 wherein the first and second sidewalls are completely non-vertical.

23. (New) The integrated circuit of claim 11 wherein the selected pitch is less than 2F.

24. (New) The integrated circuit of claim 11 wherein the selected pitch is about 1.5F.